

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Levine et al.** §
Serial No.: **Not Assigned** § Group Art Unit: **Not Assigned**
Filed: _____ § Examiner: **Not Assigned**
For: **Method and Apparatus for Maintaining** §
Performance Monitoring Structures in a §
Page Table for Use in Monitoring §
Performance of a Computer Program § Attorney Docket No.: **AUS920030488US1**

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request that the information listed on the attached Form PTO-1449 be considered by the Office during the pendency of the above entitled application, pursuant to 37 C.F.R. 1.97.

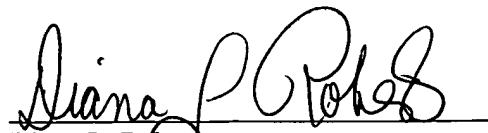
Please charge any fees necessary for prosecution of the present application to Deposit Account No. 09-0447. If any extension of time is required, such extension is hereby requested. Please charge any additional required fee for extension of time to Deposit Account No. 09-0447.

In accordance with 37 C.F.R. 1.97(h), the filing of this Information Disclosure Statement shall not constitute an admission that any information cited therein is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56(b). In the interest of full and complete disclosure to the Office, some or all of the art cited herein may not be considered by Applicant(s) or the Undersigned to be material under the new standards of materiality defined in 37 C.F.R. 1.56(b), enacted March 16, 1992, but may be material under the old standard of materiality defined in 37 C.F.R. 1.56(a), last amended on November 28, 1988, or may merely be technical background which may be of interest to the Examiner. In accordance with 37 C.F.R. 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(b) within three months of the filing date of the application, or before the mailing date of a first office action on the merits. No fee is required.

Date: 1/8/04

Respectfully submitted,



Diana L. Roberts
Registration No. 36,654
IBM Corporation
Intellectual Property Law
11400 Burnet Road
Austin, Texas 78757
(512) 823-9667

Form PTO-1449 LIST OF PRIOR ART CITED BY APPLICANT <i>(Use several sheets if necessary)</i>			ATTORNEY DOCKET NO. AUS920030488US1	SERIAL NO. Not Assigned	
			APPLICANT Levine et al.		
			FILING DATE	GROUP ART UNIT Not Assigned	
U.S. PATENT DOCUMENTS					
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE
AA	5,103,394	Apr. 7, 1992	Blasciak	395/575	Dec. 21, 1989
AB	6,330,662 B1	Dec. 11, 2001	Patel et al.	712/236	Feb. 23, 1999
AC	6,480,938 B2	Nov. 12, 2002	Vondran, Jr.	711/125	Dec. 15, 2000
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AH	6,324,689 B1	Nov. 27, 2001	Lowney et al.	717/9	Sep. 30, 1998
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BA	5,966,537	Oct. 12, 1999	Ravichandran	395/709	May 28, 1997
DATE CONSIDERED			EXAMINER		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

Form PTO-1449 LIST OF PRIOR ART CITED BY APPLICANT (Use several sheets if necessary)			ATTORNEY DOCKET NO. AUS920030488US1	SERIAL NO. Not Assigned	
			APPLICANT DeWitt, Jr. et al.		
			FILING DATE	GROUP ART UNIT Not Assigned	
U.S. PATENT DOCUMENTS					
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	INVENTOR NAME	CLASS/ SUBCLASS	FILING DATE
BB	2002/0129309	Sep. 12, 2002	Floyd et al.	714/724	Dec. 18, 2000
BC	2001/0032305	Oct. 18, 2001	Barry	712/34	Feb. 23, 2001
BD	2002/0199179	Dec. 26, 2002	Lavery et al.	717/158	Jun. 21, 2001
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BG	2002/0019976	Feb. 14, 2002	Patel et al.	717/137	May 25, 2001
FOREIGN PATENT DOCUMENTS					
EXAMINER INITIAL	DOCUMENT NO.	PUBLICATION DATE	COUNTRY	CLASS/ SUBCLASS	TRANSLATION YES NO
BH	JP2000029731	Dec. 8, 1999	Japan	G06F 9/38	X
BI	JP2000347863	Dec. 15, 2000	Japan	G06F 9/38	X
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BJ	Kikuchi, "Parallelization Assist System", Joho Shori, Vol. 34, No. 9, Sept. 1993, pp. 1158-1169.				
BK	Cohen et al., "Hardware-Assisted Characterization of NAS Benchmarks", Cluster Computing, Vol. 4, No. 3, July 2001, pp. 189-196.				
BL	Talla et al., "Evaluating Signal Processing and Multimedia Applications on SIMD, VLIW and Super Scalar Architectures", International Conference on Computer Design, Austin, Sept. 17-20, 2000, pp. 163-172.				
BM	Iwasawa et al., "Parallelization Method of Fortran DO Loops by Parallelizing Assist System", Transactions of Information Processings Society of Japan, Vol. 36, No. 8, Aug. 1995, pp. 1995-2006.				
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RELATED PATENT APPLICATIONS					
EXAMINER INITIAL	APPLICATION NO./ ATTY. DOCKET NO.	APPLICANT	TITLE		FILING DATE
BP	09/435,069 AT9-99-491	Davidson et al.	Method and Apparatus for Instruction Sampling for Performance Monitoring and Debug		Nov. 4, 1999
BQ	08/538,071 AUT919950055US1	Gover et al.	Method and System for Selecting and Distinguishing an Event Sequence using an Effective Address in a Processing System		Oct. 2, 1995
DATE CONSIDERED			EXAMINER		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					